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EXAMINER	
SONG, MATTHEW J	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/904,131	UEDA, TETSUZO	
	Examiner	Art Unit	
	Matthew J Song	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-14 and 24-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-14 and 24-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 11 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Purdes (US 4,830,984) in view of Sung (US 5,753,551) or Pey (US 6,110,811).

Purdes discloses a layer of a tensioning material on the bottom or second side of silicon substrate to counteract the tensioning force and warping effect brought on by a gallium arsenide layer applied to the first or top side of the silicon substrate (col 2, ln 55-67). Purdes also teaches reducing or eliminating warpage arising from formation of a gallium arsenide layer on a silicon substrate (col 2, ln 25-35). Purdes also teaches it is within the scope of the present invention that the layer formed on the first surface of the silicon substrate may comprise other materials other than gallium arsenide (col 5, ln 35-50) and the substrate may comprise other materials other than silicon (col 8, ln 5-20). Purdes also discloses after the layer of tensioning material is formed on the backside of the silicon substrate and treated to produce the desired warping effect by annealing at 1000°C, the gallium arsenide layer may be formed after cooling to 650°C (col 5, ln 10-25), this reads on applicant's heating step and the layered substrate exhibits bowing after being cooled down from the heating step. Purdes teaches different thermal expansion coefficients (claim 2, 3, and 7).

Purdes teaches deposition of tensioning material of metal silicide using methods known in the art (col 2, ln 10-20) and deposition of a GaAs layer at a temperature of approximately 650°C. Purdes does not teach the same growth temperature for the two layers.

In a method of depositing tungsten silicide, Sung teaches tungsten silicide is deposited using Low pressure chemical vapor deposition (LPCVD) at a temperature between 600-800°C using tungsten hexafluoride and silane as a source (col 4, ln 25-30). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Purdes by performing the GaAs deposition and metal silicide deposition at the same growth temperature because tungsten silicide is known in the art to be deposited at a temperature of 650°C, as taught by Sung. In the absence of unexpected results, performing the two depositions at the same temperature would have been obvious because the deposition temperatures for the two layers is known in the art to overlap one another.

In a method of titanium silicide deposition, Pey teaches a layer of titanium silicide is deposited by chemical vapor deposition at a deposition temperature of 650-750°C (col 3, ln 25-35 and claim 7). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Purdes by performing the GaAs deposition and metal silicide deposition at the same growth temperature because titanium silicide is known in the art to be deposited at a temperature of 650°C, as taught by Pey. In the absence of unexpected results, performing the two depositions at the same temperature would have been obvious because the deposition temperatures for the two layers is known in the art to overlap one another.

Referring to claim 11, Purdes teaches after the layer of tensioning material is formed on the backside of the silicon substrate and treated to produce the desired warping effect by

annealing at 1000°C, this reads on applicant's layered substrate which exhibits bowing. And Purdes teaches after an epitaxial gallium arsenide is formed and cooled, the structure will have a planar form (claim 1 and col 3, ln 35-65), this reads on applicant's so as to reduce bowing.

3. Claims 11, 13-14, and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (5,562,770) in view of Molnar (US 6,086,673) and Chiang (US 4,395,438).

Chen et al discloses a substrate **140** having a device layer **150** at the top and another layer of film **160** at the bottom of the substrate **140** and a substrate, which is flat when the layer **160** has negligible intrinsic stress (col 5, ln 40-67 and Fig 7A), this reads on applicant's growing an epitaxial layer on a layer substrate to reduce bowing. Chen et al also teaches providing a substrate, processing the backside of the substrate by depositing an insulating film so as to impart a convex curvature to the frontside of the substrate and growing an epitaxial layer on the substrate (claim 10 and 12). Chen et al also teaches the other applications, such as III-V compound device may be used with the instant invention (col 7, ln 1-25). Chen et al also teaches the thin film on the back surface determines the magnitude and direction of the net stress and determines if the substrate is convex or concave (col 5, ln 65 to col 6, ln 5). Chen et al also teaches minimizing the concavity of the substrate (col 6, ln 55-65). Chen et also teaches the calculation of film thickness, film stress, wafer thickness and wafer bow given the values of the other are well known (col 8, ln 1-10). Chen et al also teaches imparting a convex structure to the substrate by removing layers of a thin film or adding thin film layers to the backside of the substrate (Abstract).

Chen et al does not teach the same growth temperature for the two layers.

Chen et al teaches silicon nitride to the backside of the wafer to impart a convex curvature to the front side of the substrate (claim 1, 2, and 16) and is not particular to the process used for deposition.

In a method of depositing silicon nitride, Chiang teaches a process for forming silicon nitride on a semiconductor wafer in a low-pressure chemical vapor deposition process at a temperature of 650-900°C. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Chen et al with the conventional known method of silicon nitride (SiN) deposition taught by Chiang because Chen et al does not restrict the method used to deposit the SiN.

The combination of Chen et al and Chiang does not teach the deposition temperature of the epitaxial layer. Chen et al does teach the epitaxial film can be a III-V compound semiconductor form on a different substrate (col 7, ln 10-25).

In a method of producing a high quality III-V substrate, Molnar teaches growing an III-V nitride epitaxial layer on a foreign substrate, where the foreign substrate which can be employed includes sapphire, spinel, silicon carbide, silicon, YAG, GGG, gallium arsenide, titanium nitride, titanium carbide, ScN, InN, AlN, $In_xGa_yAl_{1-x-y}As$, $In_xGa_yAl_{1-x-y}$ or $In_xGa_yAl_{1-x-y}N$, where $0\leq x\leq 1$, $0\leq y\leq 1$,and $0\leq x+y\leq 1$. Molnar also teaches the growth substrate can also consist of layered structures composed of combinations of these materials and other such materials (col 7, ln 1-20 and Abstract). Molnar also teaches the substrate can be removed from a GaN epitaxial layer by etching, electrochemical polishing or by other suitable processes (col 11, ln 25-40). Molnar also discloses a growth temperature of 800-1250°C for GaN deposition (col 9, ln 20-30) and cooling the substrate after deposition at a rate of 1°C/min to 200°C/min under a NH_3 atmosphere (col 11,

ln 15-30). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Chen et al and Chiang by using the conventionally known process of depositing an epitaxial film taught by Molnar because Molnar does not restrict the method used to deposit the epitaxial layer.

The combination of Chen et al, Chiang and Molnar does not teach the same growth temperature for the two layer. The combination of Chen et al, Chiang and Molnar does teach SiN deposition at a temperature of 650-900°C and epitaxial deposition at 800-1250°C. In the absence of unexpected results, performing the two depositions at the same temperature would have been obvious because the deposition temperatures for the two layers is known in the art to overlap one another.

Referring to claim 11, the combination of Chen et al, Chiang and Molnar teaches a silicon substrate and an insulating layer of silicon oxide, silicon nitride or low temperature oxide (col 6, ln 5-15,50-60). Silicon and the insulating layer inherently have different thermal coefficients of expansion.

Referring to claim 24, the combination of Chen et al, Chiang and Molnar teaches removing the substrate ('673 col 11, ln 25-40).

Referring to claim 25, the combination of Chen et al, Chiang and Molnar teaches electrochemical polishing, this reads on applicant's mechanical polishing.

Referring to claim 26, the combination of Chen et al, Chiang and Molnar teaches thermally grown layers and a curvature and the substrate is convex or concave prior to substrate processing operations such as grinding, this reads on applicant's layered substrate include heating and exhibits bowing after cooling.

4. Claims 11, 13, 14, and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Molnar (US 6,086,673) in view of Purdes (US 4,830,984) and Sung (US 5,753,551).

Molnar discloses growing an III-V nitride epitaxial layer on a foreign substrate, where the foreign substrate which can be employed includes sapphire, spinel, silicon carbide, silicon, YAG, GGG, gallium arsenide, titanium nitride, titanium carbide, ScN, InN, AlN, $In_xGa_yAl_{1-x-y}As$, $In_xGa_yAl_{1-x-y}$ or $In_xGa_yAl_{1-x-y}N$, where $0\leq x\leq 1$, $0\leq y\leq 1$,and $0\leq x+y\leq 1$. Molnar also discloses the growth substrate can also consist of layered structures composed of combinations of these materials and other such materials (col 7, ln 1-20 and Abstract). Molnar also disclose the substrate can be removed from a GaN epitaxial layer by etching, electrochemical polishing or by other suitable processes (col 11, ln 25-40). Molnar also discloses a growth temperature of 800-1250°C for GaN deposition (col 9, ln 20-30) and cooling the substrate after deposition at a rate of 1°C/min to 200°C/min under a NH_3 atmosphere (col 11, ln 15-30)

Molnar is also silent to growing an epitaxial layer on a layered substrate so as to reduce bowing.

In a method of forming a planar structure, note entire reference, Purdes teaches a layer of a tensioning material on the bottom or second side of silicon substrate to counteract the tensioning force and warping effect brought on by a gallium arsenide layer applied to the first or top side of the silicon substrate (col 2, ln 55-67). Purdes also teaches reducing or eliminating warpage arising from formation of a gallium arsenide layer on a silicon substrate (col 2, ln 25-35). Purdes also teaches it is within the scope of the present invention that the layer formed on the first surface of the silicon substrate may comprise other materials other than gallium arsenide

(col 5, ln 35-50) and the substrate may comprise other materials other than silicon (col 8, ln 5-20). Purdes also teaches after the layer of tensioning material is formed on the backside of the silicon substrate and treated to produce the desired warping effect by annealing at 1000°C, the gallium arsenide layer may be formed after cooling to 650°C (col 5, ln 10-25), this reads on applicant's heating step and the layered substrate exhibits bowing after being cooled down from the heating step. Purdes teaches different thermal expansion coefficients (claim 2, 3, and 7).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the layered structure of materials with different thermal conductivities taught by Molnar with Purdes' method of reducing warpage by depositing an epitaxial layer, which counteracts a tensioning force (claim 1) to form a desirable planar structure (claim 14).

The combination of Molnar and Purdes does not teach the same growth temperature for the two layers. The combination of Molnar and Purdes merely teaches the deposition of one of the materials is 800-1250°C and is silent to the method of deposition for the tensioning material comprising a metal silicide.

In a method of depositing tungsten silicide, Sung teaches tungsten silicide is deposited using Low pressure chemical vapor deposition (LPCVD) at a temperature between 600-800°C using tungsten hexafluoride and silane as a source (col 4, ln 25-30). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Molnar and Purdes by performing epitaxial deposition and metal silicide deposition at the same growth temperature because tungsten silicide is known in the art to be deposited at a temperature of 800°C, as taught by Sung. In the absence of unexpected results, performing the two

depositions at the same temperature would have been obvious because the deposition temperatures for the two layers is known in the art to overlap one another.

Referring to claim 13-14, the combination of Molnar, Purdes and Sung teaches an III-V nitride epitaxial layer and a substrate of a layered structure of Sapphire and silicon, sapphire and an III-V nitride, sapphire and ZnO, and sapphire and SiC.

Referring to claim 24, the combination of Molnar, Purdes and Sung teaches removing the substrate ('673 col 11, ln 25-40).

Referring to claim 25, the combination of Molnar, Purdes and Sung teaches electrochemical polishing, this reads on applicant's mechanical polishing.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Molnar (US 6,086,673) in view of Purdes (US 4,830,984) and Sung (US 5,753,551) or Chen et al (US 5,562,770) in view of Molnar (US 6,086,673) and Chiang (US 4,395,438) or Purdes (US 4,830,984) in view of Sung (US 5,753,551) as applied to claims 11, 13, 14, 24-26 and 28 above, and further in view of Zheleva et al (WO 99/65068).

The combination of Molnar, Purdes and Sung or the combination of Chen, Molnar and Chiang or the combination of Purdes and Sung teaches all of the limitations of claim 12, as discussed previously, except the step of selective etching a portion of the epitaxial layer.

In a method of forming improved gallium nitride layers, note entire reference, Zheleva et al teaches an underlying gallium nitride layer **104** is grown on a SiC substrate **102** and the underlying gallium nitride layer includes a plurality of sidewalls **105** (pg 5, ln 10-35). Zheleva et al also teaches the posts **106** and trenches **107** that define the sidewalls **105** may be fabricated by selective etching (pg 6, ln 1-5). Zheleva et al also teaches the sidewalls **05** of the gallium nitride layer are laterally grown to from a lateral gallium nitride layer **108a** in the trench **107**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Molnar, Purdes and Sung or the combination of Chen, Molnar and Chiang or the combination of Purdes and Sung with Zheleva et al's selective etching of GaN to form a trench which can be used to form a relatively defect free GaN semiconductor layer (pg 2, ln 15-20).

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Molnar (US 6,086,673) in view of Purdes (US 4,830,984) and Sung (US 5,753,551) or Chen et al (US 5,562,770) in view of Molnar (US 6,086,673) and Chiang (US 4,395,438) as applied to claims 11, 13, 14, 24-26 and 28 above, and further in view of Kito et al (US 6,110,279).

The combination of Molnar, Purdes and Sung or the combination of Chen, Molnar and Chiang teaches all of the limitations of claim 25, as discussed previously. However, if there is an art recognized difference between electrochemical polishing and mechanical polish and

electrochemical polishing does not read on mechanical polishing; then it would be obvious in view of Kito et al.

In a method of producing a single crystal, note entire reference, Kito et al teaches forming a SiC single crystal layer **15** on a Silicon wafer **14** and removing the silicon wafer by a chemical technique whereby only the SiC layer remains. Kito et al also teaches a mechanical polishing step may be employed instead of the chemical technique (col 45-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Molnar, Purdes and Sung or the combination of Chen, Molnar and Chiang with Kito et al's method of removing a substrate using mechanical polishing because substitution of known equivalents for the same purpose is held to be obvious (MPEP 2144.06).

Response to Arguments

8. Applicant's arguments, see the remarks, filed 7/6/2004, with respect to Purdes and Chen et al have been fully considered and are persuasive. The rejection of claims 11 and 26 has been withdrawn. Purdes and Chen do not teach the newly added limitation of the two layers have the same growth temperature.

9. Applicant's arguments with respect to claims 11-14 and 24-26 have been considered but are moot in view of the new ground(s) of rejection.

10. Applicant's arguments filed 7/6/2004 have been fully considered but they are not persuasive.

Applicants' argument that Purdes teaches growing the two layers at two different temperatures is noted but is not found persuasive. Applicants allege that Purdes teaches titanium silicide is grown at 1000°C and GaAs is grown at 650°C. Purdes does not teach titanium silicide growth at 1000°C, as suggested by applicant. The temperature of 1000°C refers to an annealing temperature, not a growth temperature. The growth of Titanium silicide is known in the art to be between 650°C and 750°C using CVD, as taught by Pey (US 6,110,811).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Molnar is not required to teach bowing. The Purdes and Chen reference teaches bowing the substrate prior to the deposition of an epitaxial layer, note claim 15 of Purdes and claim 3 of Chen.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the prior art teaches the desirability of forming a planar epitaxial layer by reducing bowing. Furthermore, applicants admitted prior art teaches the desirability of forming planar III-V nitrides on sapphire because epitaxial III-V nitrides formed on sapphire is desirably bowed (pg 1-3 of the instant specification). The problem of bowing in III-V nitride is known and Purdes and

Chen et al teach methods of reducing bowing in epitaxial layer. Therefore, a person of ordinary skill in the art would have found it obvious to use the techniques taught by Purdes and Chen et al to reduce bowing in epitaxial layer by applying it to the conventionally known problem.

Applicants arugument that is impossible to determine the amount of bowing in Molnar is noted but is not found persuasive. Chen et al teaches the wafer bow can be calculated given the values of film thickness, film stress and wafer thickness. Also, applicants admitted prior art teaches the wafer bow can be determined by the model taught by Olsen et al (col 3, ln 5-15). Therefore, applicants argument that the wafer cannot be determined is not found persuasive because methods of determining wafer bow are conventionally known in the art.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Solomon (US 5,919,305) teaches substrate removal using etching or polishing away after an epitaxial layer is formed and the motivation is to reduce optical absorption or reduce resistive heating in the epitaxial layer by providing a better heat sink directly to the epitaxial layer (col 1 and col 2).

Lee et al (US 4,835,116) teaches III-V/Si and III-V/(Ge/Si) wafers exhibit warping due to thermal strain (col 4, ln 20-30).

Sugawara et al (US 6,232,137) teaches the thickness of layers is critical in terms of generation of crystallographic defects caused by lattice mismatch between layers (col 2, ln 60 to col 3, ln 10).

Sugawara et al (JP 10-335700) is a 102(b) equivalent to US 6,232,137.

Olsen et al ("Calculated Stresses in multilayered heteroepitaxial structures") teaches a method of calculation stress in multilayered structures, note entire reference.

Hirai et al (US 4,312,921) teaches the heating of a substrate using direct heating by an electric resistance heating, high frequency heating and the like is preferable to indirect heating because the temperature of the substrate can be controlled more precisely (col 11, ln 1-15).

Habuka (US 5,913,974) teaches heating of a semiconductor substrate uniformly over an entire area by directly heating with radiant light emitted from infrared lamps without using a susceptor reduces the time required to reach a desired temperature (col 1, ln 10-55).

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song
Examiner
Art Unit 1765

MJS

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER